In the Claims:

Please replace all previous claim listings with the following listing of claims:

1-2. (Cancelled)

3. (Currently Amended) The semiconductor memory device of Claim 4[[2]], wherein the precharge control circuit comprises:

a NAND gate which receives the precharge enable signal and the precharge delay signal; and

an inverter which inverts the output of the NAND gate.

4. (Currently Amended) A semiconductor memory device, comprising:

a memory cell array having a plurality of memory cells, a plurality of word lines, and first and second bit lines;

an address decoder which decodes a received address signal, wherein the address decoder is coupled to the plurality of word lines;

a precharge control circuit that generates a precharge signal in response to a precharge enable signal and a precharge delay signal;

a precharge unit that precharges the first and second bit lines in response to the precharge signal; and

a delay circuit which generates the precharge delay signal by delaying the precharge enable signal for a predetermined delay time, ~~The semiconductor memory device of Claim 2,~~

wherein the predetermined delay time comprises the time that it takes the word lines to become enabled in response to a transition of the decoded address signal.

5. (Currently Amended) The semiconductor memory device of Claim 4[[2]], wherein the precharge unit comprises:

a first transistor which in response to the precharge signal precharges the first bit line to a power supply voltage level;

a second transistor which in response to the precharge signal precharges the second bit line to a power supply voltage level; and

a third transistor which in response to the precharge signal equalizes the voltage of the first bit line and the second bit line.

6. (Original) The semiconductor memory device of Claim 5, wherein the first, second and third transistors are PMOS transistors.

7. (Currently Amended) A semiconductor memory device, comprising:

a memory cell array having a plurality of memory cells, a plurality of word lines, and first and second bit lines;

an address decoder which decodes a received address signal, wherein the address decoder is coupled to the plurality of word lines;

a precharge control circuit that generates a precharge signal in response to a precharge enable signal and a precharge delay signal;

a precharge unit that precharges the first and second bit lines in response to the precharge signal; and

a delay circuit which generates the precharge delay signal by delaying the precharge enable signal for a predetermined delay time, ~~The semiconductor memory device of Claim 2,~~

wherein the delay circuit comprises a NOR gate which receives the precharge enable signal and an inverter which inverts the output of the NOR gate.

8. (Currently Amended) The semiconductor memory device of Claim 4[[2]], wherein the precharge control circuit generates the precharge signal by performing a logical AND operation on the precharge enable signal and the precharge delay signal.

9. (Currently Amended) The semiconductor memory device of Claim 4,[[1]] wherein the address decoder is a row address decoder and wherein the decoded address signal comprises a row address.

10. (Original) The semiconductor device of Claim 9, wherein the precharge signal is disabled after one of the plurality of word lines is enabled in response to the decoded address signal.

11. (Currently Amended) The semiconductor device of Claim 4[[1]], wherein the precharge signal is disabled a predetermined time after the precharge enable signal is disabled.

12. (Currently Amended) A semiconductor memory device, comprising:

a memory cell array having a plurality of memory cells, a plurality of word lines, and first and second bit lines;

an address decoder which decodes a received address signal, wherein the address decoder is coupled to the plurality of word lines;

a precharge control circuit that generates a precharge signal in response to a precharge enable signal and a precharge delay signal; and

a precharge unit that precharges the first and second bit lines in response to the precharge signal;

wherein the precharge signal is disabled a predetermined time after the precharge enable signal is disabled, and

~~The semiconductor device of Claim 11,~~ wherein the precharge signal is enabled at substantially the same time that the precharge enable signal is enabled.

13-23. (Cancelled)

24. (Currently Amended) A method for pre-charging a first bit line and a second bit line of a memory cell array, the method comprising:

decoding a received address signal;

generating a precharge signal in response to a precharge enable signal and a precharge delay signal;

pre-charging the first bit line and the second bit line in response to the precharge signal; and

enabling a word line in response to the decoded address signal, wherein the precharge signal is disabled after the word line is enabled,

wherein the precharge delay signal is generated by delaying the precharge enable signal for ~~The method of Claim 23, wherein the predetermined delay time comprises~~ the time

that it takes the word lines to become enabled in response to a transition of the decoded address signal.

25. (Currently Amended) The method of Claim 24[[22]], wherein the precharge signal is disabled a predetermined time after the precharge enable signal is disabled.

26-28. (Cancelled)